REMARKS

This is a timely reply to the Official Action of August 27, 2002. In the Official Action the Examiner rejects pending claims 1-8 and 15-17 and 19-22 of the application. The grounds for rejection are traversed below. The Applicant respectfully requests that the Examiner rely on the comments regarding the patentability of the claims presented in this response and not rely on the comments regarding the patentability of the claims presented in the previous response dated May 20, 2002.

Support for Amended claims 2, 6, 18 and 22

Claims 2 and 6 have been amended to correct grammatical errors. No new matter has been added. The breadth of amended claims 2 and 6 has not been changed by this amendment.

Claim 18 has been amended and rewritten in independent form including all of the limitations of the base claim from which it depended. The breadth of amended claim 18 has not been changed by this amendment.

Claim 22 has been amended for clarity. The breadth of amended claim 22 has not been changed by this amendment.

Claims 1-8 and 15-22 remain in the application. The application comprises 5 (five) independent claims and 16 (sixteen) total claims. The application, as previously amended, comprised 4 (four) independent claims and 16 (sixteen) total claims. The additional excess claims fees have been calculated as shown in the accompanying Excess Claim Fee paper.

35 USC § 112

In the Official Action, the Examiner rejects claim 22 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the applicant regards as the invention. The Examiner asserts that it is unclear and indefinite to claim each buried conducting channel providing an electrical connection between selected ones of the plurality of spaced-apart regions in claim 19, but in dependent claim 22 to claim that said selected ones of the plurality of spaced-apart regions are not electrically connected by one of said plurality of buried conducting channels.

We have amended claim 22 to recite additional selected ones of the plurality of spaced apart regions. By adding the term "additional," we hope to clarify that the additional selected ones of the plurality of spaced-apart regions in claim 22 are not the same selected ones of the plurality of spaced-apart regions in claim 19. We submit that this amendment addresses and overcomes the Examiner's rejection of claim 22 under 35 U.S.C. 112, second paragraph.

35 USC § 103(a) - Rejection based on Choi (U.S. Patent No. 6,215,158)

Claim 1

In the Official Action the Examiner rejects the claims of the application under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,215,158 to Choi. Specifically, the Examiner asserts that Choi teaches all of the elements found in claim 1 and the recitations of "a camouflaged interconnection" and "in a manner which inhibits reverse engineering thereof" in the claim preamble are treated as non-limiting.

As noted by MPEP 2143.03, to establish a *prima facie* case for obviousness, all the claim limitations must be taught or suggested by the prior art. The Applicant respectfully asserts that Choi does not teach all of the claim limitations of claim 1.

The Examiner takes the position on page 7 of the Official Action regarding camouflaging that "the Choi reference provides the same structure as is claimed; therefore, if it is true in the present invention then it is also true in the Choi reference." Applicant respectfully disagrees that the Choi reference provides the same structure as claimed. Choi teaches in col. 3, lines 37-42 "The dielectric 190 has been patterned with openings 240, 250 to expose a portion of the first and second source regions 140, 150 respectively. A high energy beam of n-dopant may now be used to create implanted plugs 231, 232 thereby forming connections between the interconnect layer 130 and the first and second source regions 140, 150." In col. 3, lines 54-55, Choi teaches "Conductive plugs 440, 450, 460 are deposited using conventional techniques to fill the openings 240, 250, 360, respectively." Choi further teaches in col. 3, lines 58-67 that "Conductive plug 460 will ultimately provide a conventional contact for drain region 160. However, conductive plugs 440, 450 are dummy plugs, which are not to be used for contacting other parts of the semiconductor, but rather are simply used to fill the openings 240, 250 remaining after the formation of the implanted plugs 231, 232. Further connection of the first and second source regions 140, 150 to other parts of the semiconductor will be accomplished by connecting the interconnect layer 130 through a

connection not shown." We submit that the conductive plugs 440, 450, 460 are present only for two purposes. One purpose, which is served by conductive plug 460, is to provide a conventional contact. The second purpose, which is served by conductive plugs 440, 450, is to provide a contact to the underlying interconnect layer 130. Thus, a reverse engineer will see the conductive plugs 440, 450 which are not used for contacting other parts of the semiconductor and would immediately infer that a connection has been made via the interconnect layer 130. Therefore, we submit that the interconnection scheme of Choi is not camouflaged at all.

For the reasons stated above, claim 1 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 2-4 are also deemed patentable over the cited prior art through at least their dependency on claim 1.

Claim 5

As noted by MPEP 2143.03, to establish a *prima facie* case for obviousness, all the claim limitations must be taught or suggested by the prior art. The Applicant respectfully asserts that Choi does not teach all of the claim limitations of claim 5.

Claim 5 claims "at least one implanted region of opposite conductivity type being disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" (emphasis added). As discussed above, the structure of Choi does not camouflage the at least a majority of said plurality of interconnects. The Examiner is asked to point out where in Choi "at least one implanted region of opposite conductivity type being disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" is taught or suggested.

Therefore, for the reasons stated above, claim 5 is clearly distinguishable over Choi, and thus deemed to be patentable. In addition, claims 6-8 are also deemed patentable over the cited prior art through at least their dependency on claim 5.

Claim 15

New claim 15 recites, " An interconnection scheme for interconnecting two spaced-apart regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising: a first region in the integrated circuit or device disposed laterally of and in

direct contact with the two spaced-apart regions, the first region being of said common conductivity type, the first region providing a buried conducting channel for the two spaced-apart regions; and a second region of opposite conductivity type in the integrated circuit or device, said second region overlaying said first region to conceal the conducting channel." (emphasis added)

Choi does not disclose a "first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions", "the first region providing a buried conducting channel" or a "second region overlaying said first region to conceal the conducting channel".

In order to show that the present invention, as claimed in claim 15, is obvious in view of Choi, the Examiner must show how Choi teaches all of the limitations in claim 15. Thus, the Examiner is requested to show how he is interpreting Choi such that the interconnect layer 130, 231, 232 is disposed laterally of and in direct contact with the two spaced-apart regions. In addition, the Examiner is requested to show by what means the interconnect layer 130, 231, 232 of Choi is buried. Further, the Examiner is requested to show how the second doped region 121 of Choi conceals the interconnect layer 130, 232, 233. Unless the Examiner can show how Choi teaches each and every element, claim 15 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 16-17 are also deemed patentable over the cited prior art through at least their dependency on claim 15.

Claim 18

We thank the Examiner for his indication that the subject matter of claim 18 is allowable. Accordingly, we have rewritten claim 18 in independent form including all of the limitations of the base claim from which it depended. As such, claim 18 is deemed to be patentable over the art cited by the Examiner.

Claim 19

Claim 19 recites, "A interconnection scheme for interconnecting a plurality of spaced-apart regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising: a plurality of buried conducting channels, each buried conducting channel being of the common conductivity type, each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions, each buried conducing channel providing an

electrical connection between said selected ones of the plurality of spaced-apart regions; and at least one region of an opposite conductivity type in the integrated circuit or device, the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels." (emphasis added)

For reasons similar to those provided in support for the patentability of claims 1, 5 and 15, Choi does not disclose "a plurality of buried conducting channels", each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions" nor "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels".

The Examiner is asked to point out where in Choi "a plurality of buried conducting channels", each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions" or "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels" is taught or suggested.

We submit that claim 19 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 20-22 are also deemed to be patentable over the cited prior art through at least their dependency on claim 19.

Conclusion

Hence, the Applicant respectfully submits that all claims of the application are patentable over the cited references. In view of the above, reconsideration and allowance of the pending claims are respectfully solicited.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231 on

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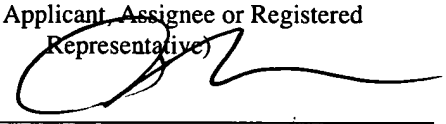
Richard P. Berg
(Name of Applicant, Assignee or Registered Representative)



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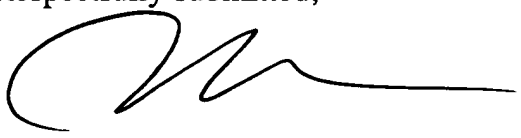
Respectfully submitted,



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APPENDIX A

2. (Once Amended) The invention of claim 1 wherein said second implanted region overlying said conducting channel has a larger area, when viewed in a direction normal to a major surface of [in] the integrated circuit or device, than has said conducting channel.

6. (Once Amended) The invention of claim 5 wherein said at least one implanted region of opposite conductivity type has a larger area than a total area of a related at least one of said conducting channels, when viewed in a direction normal to a major surface of [in] the integrated circuit or device.

18. (Once Amended) [The interconnection scheme of claim 15 further] An interconnection scheme for interconnecting two spaced-apart regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising:

a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type, the first region providing a buried conducting channel for the two spaced-apart regions;

a second region of opposite conductivity type in the integrated circuit or device, said second region overlaying said first region to conceal the conducting channel;

at least one additional spaced-apart region of the common conductivity type, said at least one additional spaced-apart region being spaced apart from the two spaced-apart regions; and

at least one additional region of the opposite conductivity type is provided in said integrated circuit or device, said at least one additional region being disposed laterally of and in direct contact with one of the two spaced-apart regions and the at least one additional spaced-apart region of the common conductivity type, wherein the one of the two spaced-apart regions and the at least one additional spaced-apart region do not have the buried conducting channel formed therebetween.

22. (Once Amended) The interconnection scheme of claim 19 further comprising at least one other region of the opposite conductivity type, the at least one other region of the opposite conductivity type being laterally disposed of and in direct contact with additional selected ones of the plurality of spaced-apart regions, wherein said additional selected ones of the plurality of spaced-apart regions are not electrically connected by one of said plurality of buried conducting channels.